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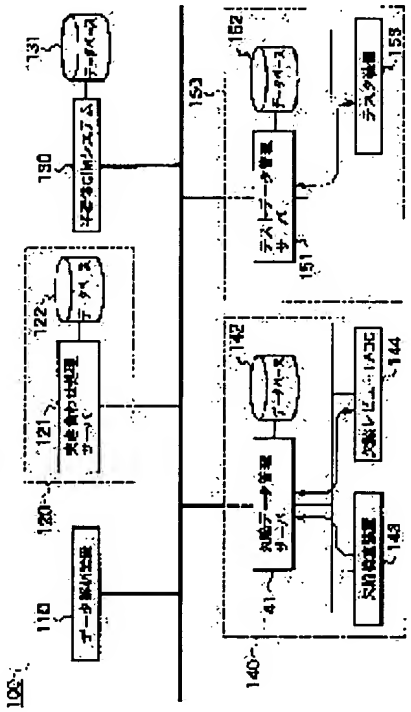
(72)Inventor : KAKINUMA HIDENORI

(54) METHOD AND SYSTEM FOR ANALYZING DEFECT

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a defect analyzing system for comprehensive defect analysis of a semiconductor wafer and improved yield in a semiconductor manufacturing process.

SOLUTION: A defect inspection means 143 which detects defects on a semiconductor wafer and generates a defect data representing defect position, defect classification data generating means 144 which references the defect data to classify the defects by size, color, and form, etc., for generating a defect classification data, tester means 153 which measures a fail bit map data representing electrical failure of the chip on a semiconductor wafer, fail bit map data processing means 151 which classifies the fail bit map data into several defective modes comprising a plurality of bits to generate a defective mode classification data before the coordinate system of the defective mode classification data is coordinate-converted into a defective data coordinate system by defective mode unit, and a matching process means 120 for defect analysis which uses the defective data, defective classification data, and coordinate-converted defective mode classification data, are provided.



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[Date of extinction of right]

* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] By detecting the defect on a semi-conductor wafer and referring to a defective inspection means to generate the defective data in which the location of the defect concerned is shown, and said defective data A classification-of-defect data generation means to classify a defect according to magnitude, a color, a configuration, etc., and to generate classification-of-defect data, A circuit tester means to measure the fail bit map data in which electric [of the chip on said semi-conductor wafer / poor] is shown, Defect Mohd classification data are created by classifying said fail bit map data into some defect Mohd who is the sets of two or more bits. The fail bit map data-processing means which carries out coordinate transformation of the system of coordinates of defect Mohd classification data to the system of coordinates of said defective data per defect Mohd, The defective analysis system characterized by having a comparison processing means to perform defective analysis using said defective data, said classification-of-defect data, and said defect Mohd classification data by which coordinate transformation was carried out.
[Claim 2] By detecting the defect on a semi-conductor wafer and referring to the defective inspection step which generates the defective data in which the location of the defect concerned is shown, and said defective data The classification-of-defect data generation step which classifies a defect according to magnitude, a color, a configuration, etc., and generates classification-of-defect data, The fail bit map data measurement step which measures the fail bit map data in which electric [of the chip on said semi-conductor wafer / poor] is shown, The defect Mohd classification step which creates defect Mohd classification data by classifying said fail bit map data into some defect Mohd who is the sets of two or more bits, The coordinate transformation step which carries out coordinate transformation of the system of coordinates of said defect Mohd classification data to the system of coordinates of said defective data per said defect Mohd, The defective analysis approach characterized by having the comparison analysis step which performs defective analysis using said defective data, said classification-of-defect data, and said defect Mohd classification data by which coordinate transformation was carried out.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the technique which the yield of a semiconductor device manufacture process raises especially about the defective analysis system which specifies the defect (Killer defect) which becomes electrically poor, and its approach by pinpointing the location which compares the defective data on a semi-conductor wafer, and the poor electric data of the chip on a semi-conductor wafer, and corresponds.
[0002]
[Description of the Prior Art] On one semi-conductor wafer, the semiconductor chip which also attains to millions - a-10 million number is increasingly carried with a rapid advance of a semiconductor integrated circuit technique in recent years. From such a background, in the semiconductor device manufacture process, it is a very important activity, and, as for detailed analysis the defect generated in a semiconductor integrated circuit, and electric [poor], a defective analysis technique is also accomplishing rapid evolution.
[0003] Although many things exist in the technique of defective analysis The defective data in which the foreign matter [on a semi-conductor wafer], defect's, etc. existence location measured with defective test equipment etc. is shown, Are measured by the electric test equipment of semiconductor memory, such as circuit tester equipment. FBM which shows the poor electric location of a semiconductor chip (Fail BitMap) It is known that the technique of specifying the defect on the semi-conductor wafer which performs comparison processing which carries out the comparison with fail bit map data, and becomes poor very electrically (Killer defect) is technique most general and powerful.
[0004] Generally, in case this comparison processing is performed, coordinate transformation is performed so that the system of coordinates of defective data and the system of coordinates of FBM data may become the same, but coordinate transformation of the defect address of FBM data is carried out for every bit, and comparison processing is usually performed after that so that the system of coordinates of FBM data may be doubled with it of defective data and it may be crowded.
[0005]
[Problem(s) to be Solved by the Invention] Thus, in the conventional defective analysis, coordinate transformation of the defect address of FBM data is carried out for every bit, and the Killer defect is specified by performing comparison processing after coordinate transformation so that the system of coordinates of FBM data may be doubled with it of defective data and it may be crowded. However, there is a technical technical problem as shown below in the defective analysis equipment and its approach to such the former.
[0006] That is, in the coordinate transformation in the defective analysis equipment and its approach to the former, in order to change the defect address of FBM data into the system of coordinates of defective data for every bit, by these days when the number of the defects who the number of bits increases by large capacity-ization of a memory device, and are generated is becoming huge, the time amount which defective analysis takes is becoming huge.
[0007] Moreover, generally, although electric [in which one defect on a semi-conductor wafer originates / poor] may lead not only to the location where the defect exists but to the defect of the direction of a word line of the defective location, or the direction of a bit line, since it has only compare defective data and FBM data simply, it cannot identify what defect the defect has cause electrically by conventional defective analysis equipment and its approach.
[0008] Furthermore, generally, although it is an activity very important when you understand the cause of generating of the defect to create classification-of-defect data by classifying a defect according to the magnitude, a color, a configuration, etc., and to perform statistical analysis of a defect since there are various magnitude, a color, and a configuration in the defect on a semi-conductor wafer By conventional defective analysis equipment and its approach, comparison processing with this classification-of-defect data and electric defect mode cannot be performed.
[0009] Although monitoring of the in-line monitoring according to a defect further again is carried out and it

performs the number of a chip with the number of defects , the number of defects of a defective mode unit , or a defect etc. , all the defects in the defective mode recognized to be a Killer defect are not very poor , and even if it can carry out monitoring of the number in Killer defective mode by conventional defective analysis equipment and its approach , the monitoring of the defect connected with electric [poor] in it cannot carry out .
[0010] This invention is made in view of the above-mentioned technical issue, and the purpose performs synthetic defective analysis on a semi-conductor wafer, and is to offer the defective analysis system which realizes improvement in the yield of a semi-conductor manufacture process.
[0011] Moreover, other purposes of this invention perform synthetic defective analysis on a semi-conductor wafer, and are to offer the defective analysis approach of realizing improvement in the yield of a semi-conductor manufacture process.
[0012]
[Means for Solving the Problem] In order to solve the above-mentioned problem, an artificer classified -FBM data into some defect modes which are the sets of two or more bits, did coordinate transformation by the data unit in defect mode, classified the - defective data which perform comparison processing with defective data according to the magnitude, a color, a configuration, etc., and suggested the defective analysis system which can perform comparison processing with FBM data using classification-of-defect data, and its approach.
[0013] The 1st description of this invention by detecting the defect on a semi-conductor wafer and referring to a defective inspection means to generate the defective data in which the location of a defect is shown, and defective data A classification-of-defect data generation means to classify a defect according to magnitude, a color, a configuration, etc., and to generate classification-of-defect data, A circuit tester means to measure the fail bit map data in which electric [of the chip on a semi-conductor wafer / poor] is shown, Defect mode classification data are created by classifying fail bit map data into some FBM(s) which are the sets of two or more bits. The fail bit map data-processing means which carries out coordinate transformation of the system of coordinates of defect mode classification data to the system of coordinates of defective data per defect mode, It is in being a defective analysis system equipped with a comparison processing means to perform defective analysis using defective data, classification-of-defect data, and the FBM data by which coordinate transformation was carried out.
[0014] It becomes possible to collect and analyze the correlation data of Killer classification-of-defect data and poor electric mode data which become poor thereby very electrically, and further, by analyzing correlation data in a detail, measures in the generating factor of a defect can be taken and improvement in the yield of a semi-conductor manufacture process can be realized.
[0015] The 2nd description of this invention by detecting the defect on a semi-conductor wafer and referring to the defective inspection step which generates the defective data in which the location of a defect is shown, and defective data The classification-of-defect data generation step which classifies a defect according to magnitude, a color, a configuration, etc., and generates classification-of-defect data, The fail bit map data measurement step which measures the fail bit map data in which electric [of the chip on a semi-conductor wafer / poor] is shown, The defect mode classification step which creates defect mode classification data by classifying fail bit map data into some defect modes which are the sets of two or more bits, The coordinate transformation step which carries out coordinate transformation of the system of coordinates of defect mode classification data to the system of coordinates of defective data per defect mode, It is in being the defective analysis approach equipped with the comparison analysis step which performs defective analysis using defective data, classification-of-defect data, and the poor FBM mode classification data by which coordinate transformation was carried out.
[0016] It becomes possible to collect and analyze the correlation data of Killer classification-of-defect data and poor electric mode data which become poor thereby very electrically, and further, by analyzing correlation data in a detail, measures in the generating factor of a defect can be taken and improvement in the yield of a semi-conductor manufacture process can be realized.
[0017] A manager terminal, the terminal for engineers, and an electronic mail transceiver means are provided, and when a semi-conductor wafer is judged to be unusual, you may make it perform the abnormality judging of whether the defect beyond a predetermined condition exists on a semi-conductor wafer, and notify that to a manager terminal and an engineer terminal in the phase where classification-of-defect data were obtained, here, using an electronic mail transceiver means.
[0018] In addition, an abnormality judging may be performed using the number of defect chips on a semi-conductor wafer.
[0019]
[Embodiment of the Invention] Hereafter, the defective analysis system concerning the operation gestalt of this invention and its approach are explained in detail using drawing 1 thru/or drawing 9 .
[0020] The defective analysis structure of a system concerning introduction and the operation gestalt of this invention is explained.
[0021] The defective analysis system 100 concerning the operation gestalt of this invention The data analysis equipment 110, defective data and classification-of-defect data which control analysis processing to be shown in drawing 1 , and FBM (Fail BitMap) The defective data control equipment 140, the FBM data, and the poor FBM

mode classification data which collect and store the comparison processor 120, defective data, and classification-of-defect data which perform comparison processing with poor fail bit map mode classification data It consists of FBM data control equipment 150 collected and stored. The comparison processor 120 The database 122 and the defective data control equipment 140 which store the comparison processing server 121 which performs comparison processing with defective data and poor FBM mode classification data, and the various data concerning comparison processing The defective test equipment 143 and defective data which collect the defective data on a semi-conductor wafer are referred to. A defect Magnitude, The defective review +ADC (Auto Defect Classification) means 144, defective data which classify according to a color, a configuration, etc. and collect classification-of-defect data, The database 142 and the FBM data control equipment 150 which store the defective data control server 141 which manages classification-of-defect data, defective data, and classification-of-defect data Poor FBM mode classification data are created from the circuit tester equipment 153 which collects the FBM data of a chip, and FBM data, and it has the database 152 which stores the test-data management server 151 which performs coordinate transformation, FBM data, and poor FBM mode classification data.
[0022] Next, the defective analysis approach concerning the operation gestalt of this invention is divided and explained to the three-stage of 1 defective data processing, 2FBM data processing, and 3 comparison processing using drawing 2 thru/or drawing 7 .
[0023] 1) In case defective data are analyzed by the defective analysis approach concerning the operation gestalt of defective data-processing this invention As shown in the flow chart Fig. shown in drawing 2 , at the beginning (defective measurement, step S101) of 1-1 defective test equipment 143 -- setting -- defective data -- measuring -- 1-2 (defective data transmission (I) --) In order to transmit step S102, next defective data to the defective data control server 141 and to review 1-3 next (defective data transmission (II), step S103) the magnitude of a defect, a color configuration, etc. Transmit the coordinate information on defective data to the defective review +ADC means 144, and it sets for 1-4, then (classification-of-defect processing, step S104) the defective review +ADC means 144. Classify a defect according to magnitude, a color, a configuration, etc., and classification-of-defect data are created. 1-5, then (classification-of-defect data transmission, step S105) classification-of-defect data are transmitted to the defective data control server 141. 1-6 Finally, (data storage, step S106), the defective data and classification-of-defect data which are used for comparison processing are created by storing defective data and classification-of-defect data in a database 142.
[0024] 2) In case FBM data are analyzed by the defective analysis approach concerning the operation gestalt of FBM data-processing this invention As shown in the flow chart Fig. shown in drawing 3 , it is 2-1 (FBM data measurement). In circuit tester equipment 153, the FBM data of the chip on a semi-conductor wafer are measured at the beginning of step S201. 2-2, next (FBM data transmission, step S202) FBM data are transmitted to the test-data management server 151. 2-3, next (a defect mode classification, step S203) FBM data are classified for every defect mode of some which are the sets of two or more bits. defect mode classification data -- creating -- 2-4 -- then, (data storage, step S204) Defect mode classification data are stored in a database 152, and it is 2-5 (coordinate transformation processing). The system of coordinates are changed into the system of coordinates of defective data for every poor step S205 mode classification data. 2-6 After performing coordinate transformation (coordinate transformation data transmission, step S206) processing by one wafer, The poor FBM mode classification data used for comparison processing are created by storing the defect mode classification data which carried out coordinate transformation in a database 152, and transmitting further the defect mode classification data by which coordinate transformation was carried out to the comparison processing server 121.
[0025] Here, I will explain the above-mentioned coordinate transformation processing briefly using drawing 4 .
[0026] The coordinate transformation processing concerning the operation gestalt of this invention defines the subset which has first the bit which constitutes FBM data as defect mode of FBM data, and begins from expressing the subset in the rectangular range. That is, let the address of the starting point P1 of a wrap rectangle, and a terminal point P2 be the range of one certain defect mode for the whole set of the bit 1 shown in drawing 5 (a). And in case coordinate transformation of the poor FBM mode data is carried out to the system of coordinates of defective data, the main coordinate (x y) and magnitude (W, D) of a rectangle field describe address description of this rectangle field so that it may double with coordinate description of a defect. Moreover, since the zero B of FBM system of coordinates generally differs from the zero A of defective system of coordinates in this case as shown in drawing 5 (b), it amends so that a mutual zero may be in agreement. By performing this processing to all the defect modes on a semi-conductor wafer, the system of coordinates of poor FBM mode classification data are changed into the system of coordinates of defective data.
[0027] By the defective analysis approach concerning the operation gestalt of comparison processing this invention, 3) Comparison processing As shown in the flow chart Fig. shown in drawing 5 , it is 3-1 (defect mode classification data reception). The poor FBM mode classification data for one wafer which analyzes are received from the test-data management server 151 at the beginning of step S301. 3-2, next (classification-of-defect data retrieval, step S302) the classification-of-defect data of the wafer equivalent to poor FBM mode classification data are searched out of a database 142. 3-3, then (comparison analysis, step S303) poor FBM mode classification data, Using defective data and classification-of-defect data, comparison processing is performed, defective

analysis is performed, and it is 3-4. Finally (data storage, step S304), it is carried out by storing a defective analysis result in a database 122.
[0028] Here, the above-mentioned comparison processing is briefly explained using drawing 6 and 7.
[0029] The comparison processing concerning the operation gestalt of this invention The tolerance fields 6 and 9 according to the configuration and magnitude of a poor FBM mode classification of the poor bit 4 and poor Rhine 7 grade are formed. It carries out by comparing defective data and classification-of-defect data, and poor FBM mode classification data, and it is considered that the defects 5 and 8 included in the tolerance fields 6 and 9 are those which are related to poor FBM (it is here). Tolerance area size shall be set as arbitration at users. And the Killer defective detail table and Killer defective detail table which indicated the result of having compared the result of comparison processing with poor FBM mode classification data for every classification of defect as shown in drawing 7 are packed as a Killer defective wafer total table which totaled per wafer, and it stores in a database 122.
[0030] Thus, since defective analysis can be performed according to the defective analysis system concerning the operation gestalt of this invention, and its approach, looking at the relation between defective data and classification-of-defect data, and poor FBM mode classification data By becoming possible to collect and analyze the correlation data in a Killer classification of defect and poor electric mode which become poor very electrically, and analyzing correlation data in a detail further The generating factor of a defect can be coped with and improvement in the yield of a semi-conductor manufacture process can be realized.
[0031] In addition, it sets to the defective analysis equipment concerning the operation gestalt of this invention, and its approach. Compute Killing Rate for every classification of defect, and it is based on the value of the Killing Rate. By setting up the weighting multiplier for an abnormality judging or yield prediction for every classification of defect (referring to drawing 9 (a)), and giving means, such as carrying out monitoring of the number of defects in consideration of a weighting multiplier The abnormalities on a semi-conductor wafer can be discovered at an early stage, and defective analysis equipment from which a defect wafer is removed, and its approach can be built by predicting the yield.
[0032] Namely, as an application of the defective analysis system concerning the operation gestalt of this invention, as shown in drawing 8 Data analysis equipment 110 is constituted from a manager terminal 111 and a terminal 112 for engineers. In furthermore, the phase where provided the electronic mail transceiver means 145 in the defective data control server 151, and classification-of-defect data were transmitted to the defective data control server 151 from the defective review +ADC means 144 The abnormality judging (monitoring) of whether the defect beyond a predetermined condition exists on a semi-conductor wafer is performed, and when a semi-conductor wafer is judged to be unusual, that is notified to the manager terminal 111 and the engineer terminal 112 using the electronic mail transceiver means 145.
[0033] Although how to judge here with the approach and the number of defect chips which are judged with the number of defects on a semi-conductor wafer although some approaches can be considered is explained as an example as the approach of the above-mentioned abnormality judging, the abnormality judging approach is not restricted to these two approaches.
[0034] The case where an abnormality judging is performed with the number of defects of a wafer is described as an example of the abnormality judging approach concerning introduction and the operation gestalt of this invention. When performing an abnormality judging with the number of defects, as shown in drawing 9 (b), the number of abnormality judging defects judged as a wafer being unusual for every classification of defect is set up first. And a weighting multiplier which was set as the number of defects of each collected classification of defect by drawing 9 (a) is applied, and announcement that the wafer concerned is unusual when it is beyond the value to which the value was set with the number of abnormality judging defects is performed. For example, although calculated value 150 is acquired by multiplying 1050 defects by the weighting multiplier 0.1 of the classification-of-defect name A when the number of abnormality judging defects shown in drawing 9 (b) is set up and the number of defects of the classification-of-defect name A is measured with 1050 pieces on a wafer Since the number of abnormality judging defects of the classification-of-defect name A is set up with 100 pieces, it is judged that the wafer concerned is unusual and a manager and an engineer come to be notified of abnormality warning.
[0035] As other examples of the abnormality judging approach concerning the operation gestalt of this invention, the case where an abnormality judging is performed with the number of defect chips is described. When performing an abnormality judging with the number of defect chips, it judges whether a certain chip becomes a defect with the number of defects, and carries out by setting up the criteria yield of a wafer in advance. That is, first, as shown in drawing 9 (c), the number of abnormality judging defects per one chip for every classification of defect is set up in advance. Supposing the number of defects of the classification-of-defect name A is 12 pieces with a certain chip at this time, 12 defective numbers will be multiplied by the weighting multiplier 0.1 of the classification-of-defect name A, and calculated value 1.2 will be acquired. Since this calculated value 1.2 is larger than one abnormality judging defect of the classification-of-defect name A, it is judged that this chip may become a defect (when we decide to perform still more nearly same processing about other classifications of defect and an abnormality judging is made even in any one of the classifications of defect, that chip shall be judged to be an

abnormality chip). And the yield of a wafer is predicted by performing abnormality judging processing of this chip to all the chips on a wafer, and extracting the number of defect chips in 1 wafer. Under the present circumstances, by preparing an abnormality criterion also in the value of the yield, if it becomes below a certain yield, defective analysis equipment which emits warning, and its approach can also be built.

[0036] Thus, including the gestalt of various operations which have not been indicated here should fully understand this invention. Therefore, this invention must be limited from this indication by only the invention specification matter concerning an appropriate claim.

[0037]

[Effect of the Invention] Since defective analysis can be performed according to the defective analysis system of this invention, looking at the relation between defective data and classification-of-defect data, and poor FBM mode classification data as stated above By becoming possible to collect and analyze the correlation data in a Killer classification of defect and poor electric mode which become poor very electrically, and analyzing correlation data in a detail further Measures in the generating factor of a defect can be taken and improvement in the yield of a semi-conductor manufacture process can be realized.

[0038] Moreover, since defective analysis can be performed according to the defective analysis approach of this invention, looking at the relation between defective data and classification-of-defect data, and poor FBM mode classification data By becoming possible to collect and analyze the correlation data in a Killer classification of defect and poor electric mode which become poor very electrically, and analyzing correlation data in a detail further Measures in the generating factor of a defect can be taken and improvement in the yield of a semi-conductor manufacture process can be realized.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the defective analysis structure of a system concerning the operation gestalt of this invention.
[Drawing 2] It is the flow chart Fig. showing the defective analysis approach concerning the operation gestalt of this invention.
[Drawing 3] It is the flow chart Fig. showing the defective analysis approach concerning the operation gestalt of this invention.
[Drawing 4] It is the mimetic diagram showing the coordinate transformation approach concerning the operation gestalt of this invention.
[Drawing 5] It is the flow chart Fig. showing the defective analysis approach concerning the operation gestalt of this invention.
[Drawing 6] It is a mimetic diagram for explaining the comparison processing concerning the operation gestalt of this invention.
[Drawing 7] It is drawing showing an example of the comparison processing result concerning the operation gestalt of this invention.
[Drawing 8] It is the block diagram showing the application of the defective analysis system concerning the operation gestalt of this invention.
[Drawing 9] It is drawing for explaining an example of the abnormality judging approach concerning the operation gestalt of this invention.
[Description of Notations]
1 Bit
2 Chip Field
3 FBM Field
4 Poor Bit
5 Eight Defect
6 Nine Tolerance
7 Poor Rhine
100 Defective Analysis System
110 Data Analysis Equipment
111 Terminal for Managers
112 Terminal for Engineers
120 Comparison Processor
121 Comparison Processing Server
122, 131, 142, 152 Database
130 Semi-conductor CIM System
140 Defective Data Control Equipment
141 Defective Data Control Server
143 Defective Test Equipment
144 Defective Review +ADC Means
145 Electronic Mail Transceiver Means
150 FBM Data Control Equipment
151 Test-Data Management Server
153 Circuit Tester Equipment
A The zero of defective system of coordinates
B The zero of FBM system of coordinates

[Translation done.]

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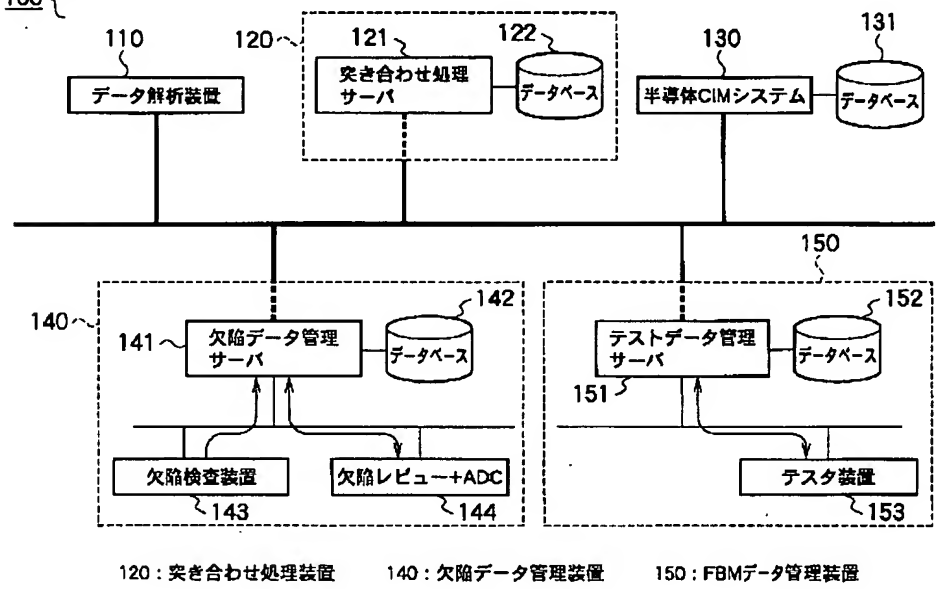
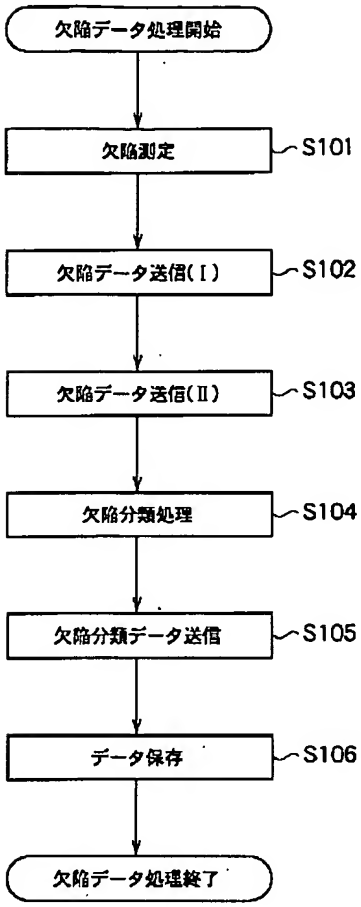
DRAWINGS

[Drawing 1]

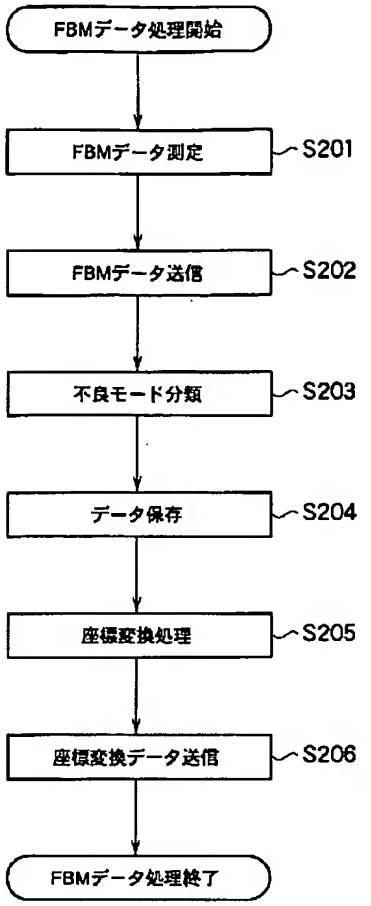


120：突き合わせ処理装置　140：欠陥データ管理装置　150：FBMデータ管理装置

[Drawing 2]

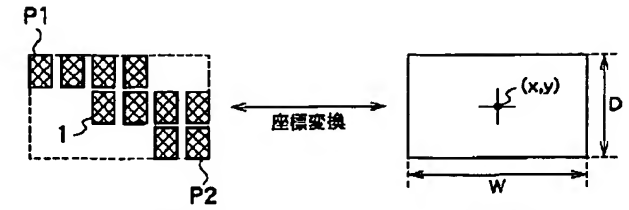

欠陥データ処理開始
欠陥測定
S101
欠陥データ送信(I)
S102
欠陥データ送信(II)
S103
欠陥分類処理
S104
欠陥分類データ送信
S105
データ保存
S106
欠陥データ処理終了

[Drawing 3]


FBMデータ処理開始
FBMデータ測定
S201
FBMデータ送信
S202
不良モード分類
S203
データ保存
S204
座標変換処理
S205
座標変換データ送信
S206
FBMデータ処理終了

[Drawing 4]

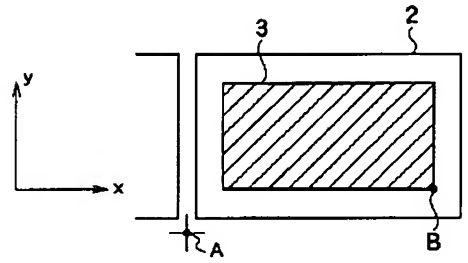
(a)



<Fail BitMap(FBM)座標系> <欠陥座標系>

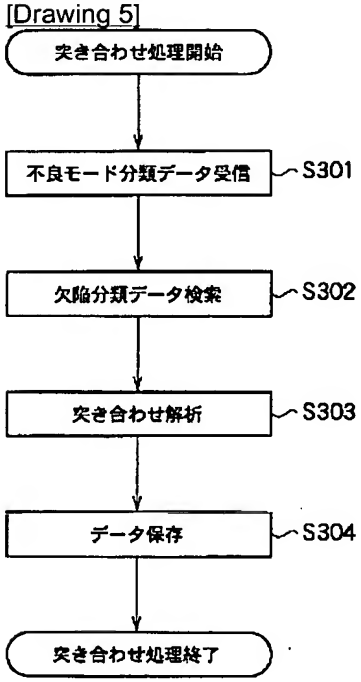
1：ビット

(b)



2：チップ領域 3：FBM領域 A：欠陥座標系の原点
B：FBM座標系の原点

[Drawing 5]



[Drawing 7]

ロット番号
ウェハー番号
工程名(欠陥測定レイヤー)
Chip座標X
Chip座標Y
欠陥中心座標x
欠陥中心座標y
欠陥分類名
FBM不良モード分類名
FBM始点Bit
FBM終点Bit

Killer欠陥詳細テーブル

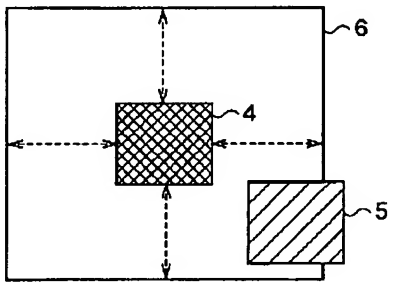
集計

ロット番号
ウェハー番号
工程名(欠陥測定レイヤー)
欠陥分類名
欠陥分類の個数
FBM不良モード分類名

Killer欠陥ウェハ集計テーブル

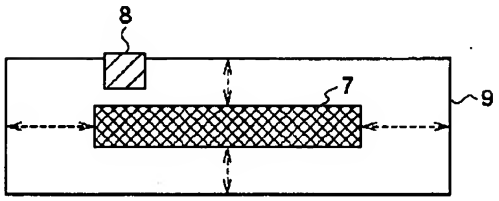
[Drawing 6]

(a)



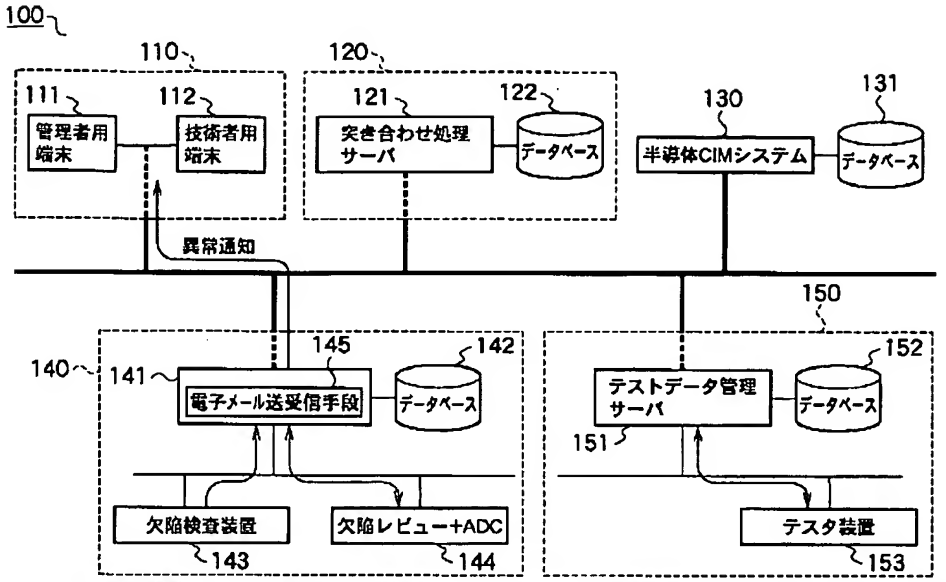
4：Bit不良　5：欠陥　6：トレランス

(b)



7：ライン不良　8：欠陥　9：トレランス

[Drawing 8]



110：データ解析装置　120：突き合わせ処理装置　140：欠陥データ管理装置　141：欠陥データ管理サーバ
150：FBMデータ管理装置

[Drawing 9]
(a)

欠陥分類名	Killing Rate	重み
A	10%	0.1
B	30%	0.3
C	50%	0.5
D	40%	0.4

(b)

欠陥分類名	1ウェハー中の異常判定欠陥数
A	100個以上
B	80個以上
C	20個以上
D	30個以上

(c)

欠陥分類名	1チップ中の異常判定欠陥数
A	1 個以上
B	4個以上
C	2個以上
D	3個以上

[Translation done.]